REMARKS

This paper is responsive to non-final Office Action dated January 14, 2004. Claims 1-39 were examined. Claims 25 and 27 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 1, 3, 4, 6, 7, 15-20, 23, 31, and 35-39 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,623,185 to Peragine. Claims 13, 33, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Peragine. Claims 2, 5, 8-12, 14, 21, 22, 24, 26, 28, 29, 30 and 32 are objected to for depending from a rejected base claim.

Proposed Changes to the Drawings

Figure 18 has been changed to couple register 1205 to node 512 and to couple delay path 1815 to clock signal 514, consistent with the specification. No new matter has been added.

Claim Rejections Under 35 U.S.C. § 112

Claims 25 and 27 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claim 25 recites the limitation "the first data path" in line 1. The Office Action points out that there is insufficient antecedent basis for this limitation in the claim. Claim 25 has been amended to depend from claim 24 to provide proper antecedent basis.

Claim 27 recites the limitation "the second data path" in line 1. The Office Action points out that there is insufficient antecedent basis for this limitation in the claim. Claim 27 has been amended to depend from claim 24 to provide proper antecedent basis.

Claim Rejections Under 35 U.S.C. § 102(e)

Claims 1, 3, 4, 6, 7, 15-20, 23, 31, and 35-39 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,623,185 to Peragine. Claim 1 has been amended to replace --acquired-- with "locked to." In addition, claim 1 has been amended to recite

> adjusting an output frequency of a variable frequency oscillator circuit in response to a determination that

> the PLL has not locked to the timing of the input data stream,

which Applicant respectfully maintains is patentable over the art of record. The Office Action states that "[a]nd based on this loss of signal output the oscillator would instantaneously be varied or changed," but fails to point out where Peragine provides that teaching. Applicant respectfully maintains that Peragine provides no such teaching or suggestion that the oscillator output is varied based on the LOS condition. Instead, Peragine is directed to detecting a LOS condition and not trying to achieve lock in response to detection of the LOS condition. In fact, Peragine teaches that "the 32.77 MHz VCXO clock signal is present even during an LOS event. Additionally, because it is a crystal oscillator, the frequency does not change significantly from that in the locked state. Thus, in an embodiment, a consistent sampling window can be obtained by using a VCXO." (Col. 3, lines 57-62) Thus, Peragine fails to teach or suggest adjusting an output frequency of a variable frequency oscillator circuit in response to a determination that the PLL has not locked to the timing of the input data stream, as recited in amended claim 1. Accordingly, Applicant respectfully requests that the rejection of claim 1 and all claims dependent thereon be withdrawn.

Claim 7 has been cancelled.

Claim 16 has been amended to recite

> means for adjusting an output frequency of a variable frequency oscillator circuit in response to a determination that the PLL has not recovered the timing.

Applicant respectfully maintains that Peragine, alone or in combination with other references of record, fails to teach or suggest adjusting an output frequency of a variable frequency oscillator circuit in response to a determination that the PLL has not recovered the timing, as recited by amended claim 16. The Office Action states that "[a]nd based on this loss of signal output the oscillator would instantaneously be varied or changed." Applicant respectfully maintains that Peragine provides no such teaching or suggestion that the oscillator output is varied based on the

LOS condition. Instead, Peragine is directed to detecting a LOS condition and not trying to achieve lock in response to detection of the LOS condition. Thus, Peragine fails to teach or suggest adjusting an output frequency of a variable frequency oscillator circuit in response to a determination that the PLL has not recovered the timing, as recited in amended claim 16. Accordingly, Applicant respectfully requests that the rejection of claim 16 and all claims dependent thereon be withdrawn.

Claim 17 has been amended to correct a typographical error.

Regarding claim 19, Applicant respectfully maintains that Peragine, alone or in combination with other references of record, fails to teach or suggest

> varying an output of a variable oscillator until transitions of the input data stream occurring in a predefined phase zone of a sample clock sampling the input data stream occur below an acceptable rate,

as recited in claim 19. The Office Action states that "[a]nd based on this loss of signal output the oscillator would instantaneously be varied or changed." Applicant respectfully maintains that Peragine provides no such teaching or suggestion. Accordingly, Applicant respectfully requests that the rejection of claim 19 and all claims dependent thereon be withdrawn.

Regarding claim 23, Applicant respectfully maintains that Peragine, alone or in combination with other references of record, fails to teach or suggest

> a control circuit, responsive to the indication that lock is not achieved, to vary the output of the variable oscillator circuit,

as recited by claim 23. The Office Action states that "[a]nd based on this loss of signal output the oscillator would instantaneously be varied or changed." Applicant respectfully maintains that Peragine provides no such teaching or suggestion. Accordingly, Applicant respectfully requests that the rejection of claim 23 and all claims dependent thereon be withdrawn.

Claim 36 has been amended to recite

adjusting an output frequency of a variable oscillator circuit according to whether transitions of the input data stream occur below a predetermined rate in a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream,

which Applicant respectfully maintains is patentable over the art of record. The Office Action states that "[a]nd based on this loss of signal output the oscillator would instantaneously be varied or changed." Applicant respectfully maintains that Peragine provides no such teaching or suggestion. Accordingly, Applicant respectfully requests that the rejection of claim 36 and all claims dependent thereon be withdrawn.

Claim 37 has been amended to recite

means coupled to the variable oscillator for adjusting an output frequency of the variable oscillator circuit based at least in part on whether the phase-locked loop has locked to an input data stream,

which Applicant respectfully maintains is patentable over the art of record. The Office Action states that "[a]nd based on this loss of signal output the oscillator would instantaneously be varied or changed." Applicant respectfully maintains that Peragine provides no such teaching or suggestion. Accordingly, Applicant respectfully requests that the rejection of claim 37 and all claims dependent thereon be withdrawn.

Claim 38 has been amended to recite

a method comprising <u>adjusting an output frequency of a variable oscillator circuit</u> according to whether transitions, occurring in a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream of the input data stream, occur below a predetermined rate,

which Applicant respectfully maintains is patentable over the art of record. The Office Action states that "[a]nd based on this loss of signal output the oscillator would instantaneously be varied or changed." Applicant respectfully maintains that Peragine provides no such teaching or suggestion. Accordingly, Applicant respectfully requests that the rejection of claim 38 and all claims dependent thereon be withdrawn.

Claim 39 has been amended to depend from claim 38.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 13, 33, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Peragine. Applicant respectfully maintains that these claims depend from allowable base claims and are allowable for at least this reason. Accordingly, Applicant respectfully requests that the rejection of claims 13, 33, and 34 claims be withdrawn.

Claim 13 has been amended to depend from claim 1.

Claim 34 is amended to correct a typographical error.

Allowable Subject Matter

Applicant appreciates the indication of allowable subject matter in claims 2, 5, 8-12, 14, 21, 22, 24, 26, 28-30, and 32. Applicant respectfully maintains that these claims depend from allowable base claims and are allowable for at least this reason.

Claim 2 has been put in independent form. In addition, claim 2 has been amended to replace --is locked to-- with "has acquired."

Claim 5 has been put in independent form. In addition, claim 5 has been amended to replace --acquired-- with "locked to."

Claim 8 has been amended to depend from claim 1.

In summary, claims 1-6 and 8-39 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited.

Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

☐ deposited with the US Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

☐ facsimile transmitted to the US Patent and Trademark Office.

_____ _____
Date

EXPRESS MAIL LABEL: EV436536406US

Respectfully submitted,

Nicole Teitler Cave, Reg. No. 54,021
Attorney for Applicant(s)
(512) 338-6315
(512) 338-6301 (fax)

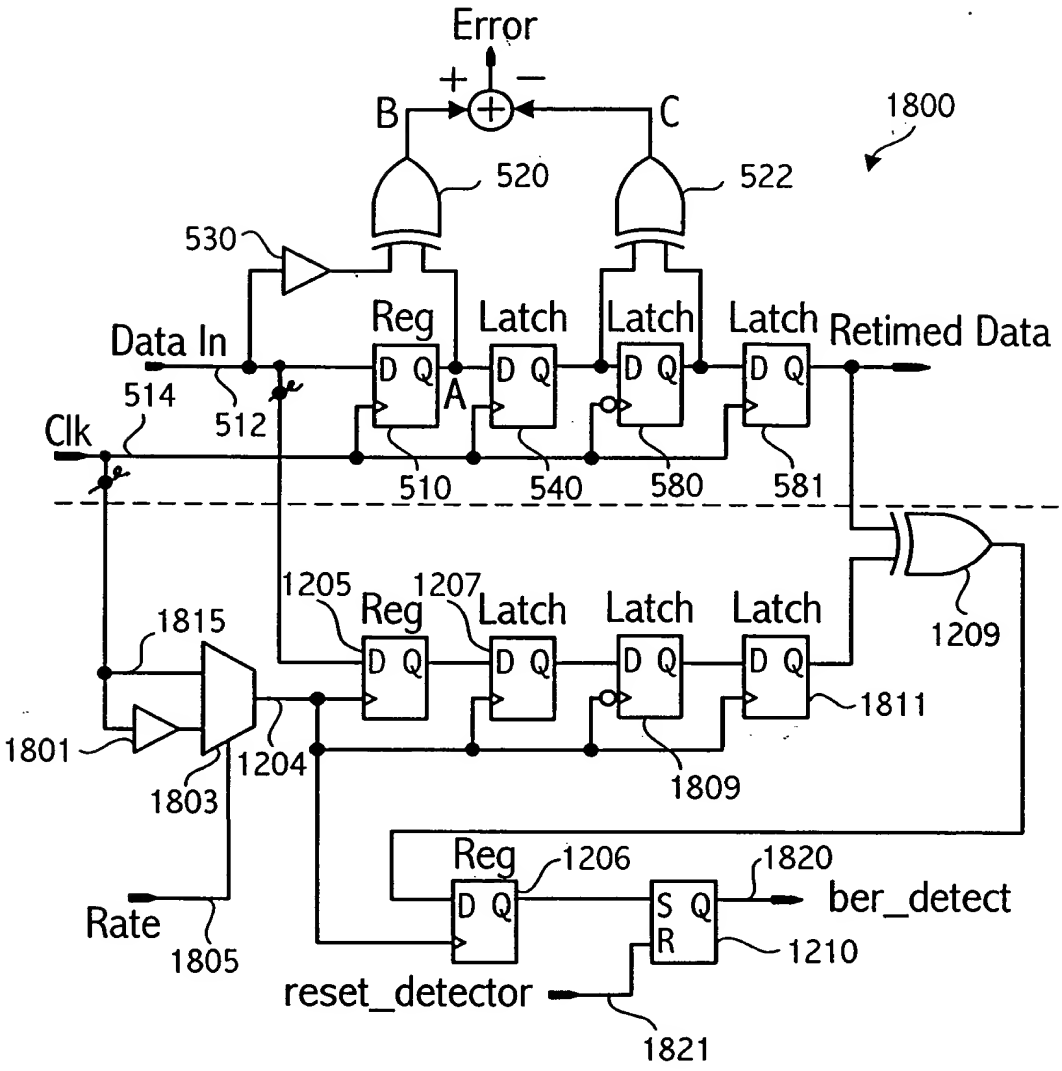

FIG. 18